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SE-6789

B. E. - III (Sem. VI (EC/ECC) Examination

April / May – 2011

Digital Microelectronic & Circuits (EC 505 EC/ECC)

Time :3 Hours] [Total Marks : 100

Instructions :

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ B. E. - 3 (SEM. 5) (EC/ECC)

Name of the Subject :

☛ Digital Microelectronic & Circuits (EC 505 EC/ECC)

☛ Subject Code No. : 6 7 8 9 ☛ Section No. (1, 2,.....) : NIL

Seat No. :

Student's Signature

1. **Attempt all questions.**
2. **Figure in the right indicate marks.**
3. **Assume suitable data if required.**

1

(a) Attempt following **(14)**

1. Define the following terms
   (a) Current sinking (b) Loading factor
2. Define the following terms
   (a) VoL (b) ViL
3. Draw the circuit diagram of RTL EX-OR gate.
4. State the disadvantages of DCTL.
5. When propagation delay referred as hazards. Describe the technique to reduce propagation time.
6. Compare TTL and DTL logic family.
7. Define the following terms
   (a) Fan out (b) Noise margin

(b) Fill in the blank **(06)**

1. The maximum fan out of RTL buffer as per the manufacturer specification is N=_____.
2. The fanout of the standard TTL IC is _____.
3. I^2L is the modify version of the _____.
4. The typical value of Rc is _____ or _____ in Integrated form of DTL gate.
5. Noise immunity Δ0 represented by _____ and Δ1 represented by_____.
6. _____ logic family having highest noise margin.

2 Attempt the following

(a) Explain Input VI characteristics of TTL gate **(05)**

(b) Draw the circuit diagram to show how DCTL gate can connected to perform the logic operation AND and NOT. **(03)**

(c) Briefly explain Integrated Injection Logic. **(07)**

OR

2 Attempt the following

(a) Explain Input Output characteristics of DTL gate with necessary diagram. **(07)**

(b) Draw and explain transfer characteristics of ECL OR gate. **(08)**

3 Write Short notes (any three) **(15)**

(a) Multiemitter Transistor.

(b) Schottky TTL.

(c)Physical layout of IIL.

(d) ECL NOR gate.

4 (a) Answer **any five** of the following in short. (Two marks each) **[10]**

1. Compare BJT and CMOS for speed of operation and power dissipation.
2. Differentiate static and dynamic memory.
3. What do you mean by domino logic circuit?
4. Give example of volatile and non volatile memory.
5. Draw CMOS inverter.
6. Discuss W/L ratio of MOS transistor.

4 (b) Using NMOS logic family and CMOS logic family realize Boolean function **[05]**

$Y = \overline{A + BC}$

4 (c) Classify semiconductor memory. **[05]**

5 Answer **any three** of the following **[15]**

1. Draw and explain BiCMOS NAND gate.
2. Explain static memory with diagram.
3. Discuss dynamic shift register with appropriate diagram.
4. Discuss construction of ROM (Read only memory)
5. A microcomputer system has total 16Kbytes of memory. Basic memory module is available in 4096 words each of 4-bit capacity. Sketch memory organization for above system. How many Address & Data lines are needed for system

6 Answer **any three** of the following **[15]**

1. Show how 1 bit full adder circuit can be implemented using PLA?
2. Write short note on FPGA.
3. Explain gate array approach for VLSI design with diagram.
4. With diagram explain VLSI circuit design.
5. Compare CMOS and BiCMOS logic family.